<u>PATENT</u>

Appl. No. 10/751,283 Amdt. dated January 19, 2006 Amendment under 37 CFR 1.116 Expedited Procedure Examining Group 2819

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

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1. (previously presented) A programmable logic device, comprising a plurality of logic elements and a routing structure, wherein the routing structure comprises a plurality of routing lines, and wherein each routing line comprises:

a plurality of first OR gates, each first OR gate having at least a first input connected to a respective one of said logic elements in a first group of said logic elements, and each first OR gate except a final first OR gate in said line having an output connected to a second input of a respective succeeding one of said first OR gates, such that a signal from one of said logic elements in the first group of logic elements appears on an output of the final first OR gate in said line; and

a return line, comprising a plurality of drivers connected in series, each of said drivers having a connection to a respective one of a plurality of said logic elements in a second group of logic elements, such that the signal appearing on said output of the final first OR gate it said line may be passed to said plurality of logic elements in the second group of logic elements.

- 2. (original) A programmable logic device as claimed in claim 1, wherein the first group of logic elements and the second group of logic elements are mutually exclusive.
- 3. (original) A programmable logic device as claimed in claim 1, wherein the first group of logic elements and the second group of logic elements contain at least one logic element in common.
- 4. (original) A programmable logic device as claimed in claim 1, wherein the logic elements in said programmable logic device are arranged in an array, the array comprising rows and columns of logic elements.